



AF 72

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

EDGARR R. ZUNIGA-ORTIZ ET AL.

Serial No. 10/769,699 (TI-33535.1)

Filed March 2, 2004

For: BUMPERLESS WAFER SCALE DEVICE AND BOARD ASSEMBLY

Art Unit 2814

Examiner Hoai V. Pham

Customer No. 23494

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF MAILING OR TRANSMISSION UNDER 37 CFR 1.8

I hereby certify that the attached document is being deposited with the United States Postal Service with sufficient postage for First Class Mail in an envelope addressed to Director of the United States Patent and Trademark Office, P.O. Box 1450,, Alexandria, VA 22313-1450 or is being facsimile transmitted on the date indicated below:

5-18-07

Jay M. Cantor, Reg. No. 19,906

BRIEF ON APPEAL

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences.

STATUS OF CLAIMS

This is an appeal of claims 27 to 32, all of the rejected claims. No claims have been allowed and claims 1 to 26 were the subject of the parent application which is now Patent No. 6,768,210. Please charge any costs to Deposit Account No. 20-0668.

STATUS OF AMENDMENTS

An amendment was not filed after final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 31, as depicted in Fig. 2, relates to a method for fabricating a semiconductor assembly and includes the steps of (a) providing a semiconductor chip (201, page 10, line 30ff) having a planar active surface including an integrated circuit (201a, page 10, line 32 and page 11, line 1), the integrated circuit having metallization patterns (202, page 11, line 5) including a plurality of contact pads at the planar active surface (202a, page 11, line 6), (b) providing a protective overcoat over the planar active surface (203, page 11, line 7ff), the protective overcoat including windows exposing the plurality of contact pads (photoresist window defining contact pad 202a, page 11, lines 12ff), the windows having sidewalls, (c) providing an added conductive region having at least one conductive layer on the metallization pattern covering and *conformal to each of the contact pads* (205, page 12, line 13ff), the sidewalls of the windows and a portion of the protective overcoat surrounding the windows, the added conductive region having a planar outer surface, the outer surface of the added conductive region suitable to form metallurgical bonds without melting (206, page 12, line 29ff, 207, page 15, line 3ff)), (d) providing an assembly board having a plurality of planar, metallurgically bondable terminal pads in a distribution aligned with the distribution of the contact pads, aligning the added metallization and the board pads so that each of said contact pads is connected to a corresponding board terminal pad, and metallurgically bonding the added metallization and the board pads without melting the outer surface of the added conductive region (page 15, line 13ff and page 18, line 4ff).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether the objection to claim 31 is proper.

Claims 27, 28 and 30 to 32 were rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al. (U.S. 6,709,901).

Claims 29 was rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. in view of Akram et al. (U.S. 6,617,687).

ARGUMENT

It is initially noted that claim 31 was objected to (not rejected) in view of the use of the term “windows” as opposed to –window—as suggested by the examiner. It is respectfully submitted that “windows” is the correct term since there is a window for each contact pad. Only one of the contact pads is shown in Fig. 2, though it is understood and well known in the art that the semiconductor chip has a plurality of contact pads. Furthermore, plural contact pads are so stated at page 11, lines 5 and 6.

Claims 27, 28 and 30 to 32 were rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al. (U.S. 6,709,901). The rejection is without merit.

It is basic that, for a claim to be rejected under section 102, each and every feature of the claim must be found in a single reference. This is clearly not the case herein.

Claim 31 requires, among other features, providing an added conductive region on the metallization pattern covering and conformal to each of the contact pads, the sidewalls of the windows and a portion of the protective overcoat surrounding the windows, the added conductive region having a planar outer surface, the outer surface of the added conductive region suitable to form metallurgical bonds without melting. No

such feature is taught or suggested by Yamazaki et al. either alone or in the combination as claimed. In fact, the requirement for conformality is conveniently omitted from the argument presented by the examiner.

With reference to Fig. 10(B) of Yamazaki et al., the figure referred to in the rejection, it is clear that the structure does not meet the requirements of the method as claimed. The region 230 does not meet the requirements of claim 31 as set forth in the above paragraph since it is clearly not conformal to each of the contact pads, the sidewalls of the windows and a portion of the protective overcoat surrounding the windows, the added conductive region having a planar outer surface, the outer surface of the added conductive region suitable to form metallurgical bonds without melting.

The above described feature is discussed at page 4, lines 10ff where it is stated “[e]ach of these contact pads has an added conductive layer on the circuit metallization. This added layer has a conformal surface adjacent the chip and a planar outer surface, and this outer surface is suitable to form metallurgical bonds without melting (underline not in original)”. No such step nor its benefits are taught or even remotely suggested by Yamazaki et al.

Claim 31 further requires providing an assembly board having a plurality of planar, metallurgically bondable terminal pads in a distribution aligned with the distribution of the contact pads, aligning the added metallization and the board pads so that each of the contact pads is connected to a corresponding board terminal pad and metallurgically bonding the chip metallization and the board pads without melting the outer surface of the added conductive layer. No such features are taught or suggested by Yamazaki et al. either alone or in the combination as claimed.

By the above claimed procedure, the board terminal pad is connected directly to the bond pad, thereby eliminating the required conductive particle 227 or barrier layer 229 of Yamazaki et al.

Claims 27, 28, 30 and 32 depend from claim 31 and therefore define patentably over Yamazaki et al. for at least the reasons stated above with reference to claim 31.

In addition, claim 27 further limits claim 31 by requiring that the step of depositing be selected from a group consisting of sputtering, evaporating, and plating. No such combination is taught or suggested by Yamazaki et al.

Claim 28 further limits claim 31 by requiring that the step of fabricating a planar outer surface of the added conductive layer comprise the step of depositing at least one added conductive layer by electroless plating. No such combination is taught or suggested by Yamazaki et al.

Claim 30 further limits claim 31 by requiring that the step of fabricating a planar outer surface of the added conductive layer comprise the step of depositing at least one added conductive layer by using the method of support by islands of protective overcoat. No such combination is taught or suggested by Yamazaki et al.

Claim 32 further limits claim 31 by requiring that the bonding comprise one of direct welding by metallic interdiffusion, attaching including solder paste and attaching including a conductive adhesive. No such combination is taught or suggested by Yamazaki et al.

Claim 29 was rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. in view of Akram et al. (U.S. 6,617,687). The rejection is without merit.

Claim 29 depends from claim 31 and therefore defines patentably over the applied references for at least the reasons presented above with reference to claim 31 since Akram et al. fails to overcome the deficiencies of Yamazaki et al. as discussed above.

Claim 29 further limits claim 31 by requiring that the step of fabricating a planar outer surface of the added conductive region comprise the step of depositing a second of at least one added conductive layer by screen printing. No such combination is taught or suggested by Yamazaki et al., Akram or any proper combination of these references.

CONCLUSIONS

For the reasons stated above, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,



Jay M. Cantor
Reg. No. 19906
(301) 424-0355
(972) 917-5293

CLAIMS APPENDIX

The claims on appeal read as follows:

27. The method according to Claim 31 wherein said step of providing an added conductive region is selected from a group consisting at least in part of sputtering, evaporating, and plating.

28. The method according to Claim 31 wherein said step of fabricating a planar outer surface of said added conductive region comprises the step of depositing a second of at least one added conductive layer by electroless plating.

29. The method according to Claim 31 wherein said step of fabricating a planar outer surface of said added conductive region comprises the step of depositing a second of at least one added conductive layer by screen printing.

30. The method according to Claim 31 wherein said step of fabricating a planar outer surface of said added conductive region comprises the step of depositing a second of at least one added conductive layer by using the method of support by islands of protective overcoat.

31. A method for fabricating a semiconductor assembly comprising the steps of:

providing a semiconductor chip having a planar active surface including an integrated circuit, said integrated circuit having metallization patterns including a plurality of contact pads at said planar active surface,

providing a protective overcoat over said planar active surface, said protective overcoat including windows exposing said plurality of contact pads, said windows having sidewalls;

providing an added conductive region having at least one conductive layer on said metallization pattern covering and conformal to each of said contact pads, said sidewalls of said windows and a portion of said protective overcoat surrounding said windows, said added conductive region having a planar outer surface, said outer surface of said added conductive region suitable to form metallurgical bonds without melting;

providing an assembly board having a plurality of planar, metallurgically bondable terminal pads in a distribution aligned with the distribution of said contact pads;

aligning said added metallization and said board pads so that each of said contact pads is connected to a corresponding board terminal pad; and

metallurgically bonding said added metallization and said board pads without melting said outer surface of said added conductive region.

32. The method according to Claim 31 wherein said bonding comprises one of the following assembly techniques:

direct welding by metallic interdiffusion;

attaching including solder paste;

attaching including a conductive adhesive.



EVIDENCE APPENDIX

N/A

RELATED PROCEEDINGS APPENDIX

N/A